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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,792	BERKOVICH, EFRAIM	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 07/27/2004 have been fully considered but they are not persuasive.

The Applicant contends, "As previously detailed, the prior art fails to describe or suggest the pairwise combination of indices, this distinction previously emphasized by the embodiment of the invention to which previously presented claims 22, 24 and 26 are directed and now further emphasized by the present amendment to the independent claims".

The Examiner disagrees and asserts that Arnold teaches an inverse fault-tolerant decoder implemented for an error-correction code (Note: decoding substantially performs the inverse of encoding since decoding extracts data from originally encoded data and hence is substantially the inverse of encoding; in addition, the Decoder in Figure 1 of Arnold is designed to perform the inverse operation of decoding in order to retrieve fault-tolerant data hence is an inverse fault-tolerant decoder) configured to transform a data vector into a plurality of predetermined index values, each of said index values specifying a location within a first address space (the data vector on line 128 in Figures 1 and 3A in Arnold are transformed into Hash indices HF1-HFH whereby H=3 in Figure 3A); combining pairs of said index values to form corresponding pairwise combined hash indices (Figures 3A and 5 in Arnold teach that the combination of HF1-HFH form

combined hash indices for looking up data in 4kx16 ROS; in the case that H=2 the pair HF1-HF2 form a pairwise combined hash indices for looking up data in a pair of 4kx16 ROS), each of said pairwise combined hash indices specifying a location within a second address space, said second address space being greater than said first address space (in the case that H=2 the pair HF1-HF2 form a pairwise combined hash indices for looking up data in a pair of 4kx16 ROS whereby the size of the Address space for the pair HF1-HF2 is 2 times the size of the Address space for either HF1 or HF2); and data storage configured as a hash table addressable throughout said second address space, said hash table referencing indexed data corresponding to said combined hash indices (in the case that H=2 the pair HF1-HF2, a pair of 4kx16 ROS form a data storage configured as a hash table addressable throughout said second address space, said hash table referencing indexed data corresponding to said combined hash indices).

Specification

2. The disclosure is objected to because of the following informalities:

Nowhere does the specification teach "**combinational logic**" to combine pairs of said index values to form corresponding pairwise combined hash indices as claimed in claims 1, 6, 7, 15, 19 and 20.

Paragraphs [0105]-[0106] in the Applicant's specification instead teach combining pairs of said index values to form corresponding pairwise combined hash indices.

Nowhere does the specification teach "each of said pairwise combined hash indices **specifying a location within a second address space**" as claimed in claims 1, 8 and 15. Note: Paragraph [0106] in the Applicant's specification states that ordered pairs are used as Access pairs "into a table as shown in Figure 9". However, Figure 9 is not a table and Figure 9 instead shows that pairs of indices are selected in Step 205 and used to generate hash keys

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-8 and 15-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites, "**combinational logic** configured to combine pairs of said index values to form corresponding pairwise combined hash indices" [Emphasis Added].

Claim 6 recites, "**combinational logic** configured to combine pairs of said index values to form corresponding pairwise combined hash indices" [Emphasis Added].

Claim 7 recites, "**combinational logic** configured to combine pairs of said index values to form corresponding pairwise combined hash indices" [Emphasis Added].

Claim 15 recites, "**combinational logic** configured to combine pairs of said index values to form corresponding pairwise combined hash indices" [Emphasis Added].

Claim 19 recites, "**combinational logic** configured to combine pairs of said index values to form corresponding pairwise combined hash indices" [Emphasis Added].

Claim 20 recites, "**combinational logic** configured to combine pairs of said index values to form corresponding pairwise combined hash indices" [Emphasis Added].

Nowhere does the specification teach "**combinational logic**" to combine pairs of said index values to form corresponding pairwise combined hash indices. Paragraphs [0105]-[0106] in the Applicant's specification instead teach combining pairs of said index values to form corresponding pairwise combined hash indices.

Note: claims 21-26 also suffer from the same issues as claims 1, 8 and 15, i.e., there is no support for the term "**combinational logic**".

Claim 1 recites, "each of said pairwise combined hash indices **specifying a location within a second address space**, said second address space being greater than said first address space" [Emphasis Added].

Claim 8 recites, "each of said pairwise combined hash indices **specifying a location within a second address space**, said second address space being greater than said first address space" [Emphasis Added].

Claim 15 recites, "each of said pairwise combined hash indices **specifying a location within a second address space**, said second address space being greater than said first address space" [Emphasis Added].

Nowhere does the specification teach "each of said pairwise combined hash indices **specifying a location within a second address space**". Note: Paragraph [0106] in the Applicant's specification states that ordered pairs are used as Access pairs "into a table as shown in Figure 9". However, Figure 9 is not a table and Figure 9 instead shows that pairs of indices are selected in Step 205 and used to generate hash keys.

The Examiner assumes the following was intended in claims 1, 8 and 15: -- combining pairs of said index values to form corresponding pairwise combined hash indices--.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-6, 8-13, 15-19 and 21-26 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01.

Claim 1 recites "A data dictionary" in the preamble. Claim 6 recites "A data dictionary" in the preamble. Claim 7 recites "A data dictionary" in the preamble. Claim 8 recites "A method of accessing a dictionary" in the preamble. Claim 13 recites "A method of accessing a dictionary" in the preamble. Claim 14 recites "A method of accessing a dictionary" in the preamble. Claim 15 recites "A data dictionary" in the preamble. Claim 19 recites "A data dictionary" in the preamble. Claim 20 recites "A data dictionary" in the preamble. The omitted elements are: the relationship between a data dictionary and the limitations in the body of claim 1.

Claim 6 recites "identify all possible offsets from adjacent decoding spheres of said error-correction code until said combinations **fill in all bit positions** corresponding to said data vector such that centers of said adjacent decoding spheres correspond to said index values" [Emphasis Added]. What bit positions are being filled in? Note: bit positions generally refer to the position of a bit in a data stream or a group of data bits, yet nowhere does the claim specify any data stream or a group of data bits related to the bit position.

Claim 7 recites "combines said centers of said adjacent decoding spheres with said center of said central index decoding sphere to form **pairs of indexes**" [Emphasis Added]. The relationship between index values, pairwise combined hash indices in claim and pairs of indices is not clear. Are pairs of indexes the same as pairwise combined hash indices or are the some other index?

Claim 13 recites "identify all possible offsets from adjacent decoding spheres of said error-correction code until said combinations **fill in all bit positions**

corresponding to said data vector such that centers of said adjacent decoding spheres correspond to said index values" [Emphasis Added]. What bit positions are being filled in? Note: bit positions generally refer to the position of a bit in a data stream or a group of data bits, yet nowhere does the claim specify any data stream or a group of data bits related to the bit position.

Claim 14 recites "combines said centers of said adjacent decoding spheres with said center of said central index decoding sphere to form **pairs of indexes**" [Emphasis Added]. The relationship between index values, pairwise combined hash indices in claim and pairs of indices is not clear. Are pairs of indexes the same as pairwise combined hash indices or are the some other index?

Claim 19 recites "identify all possible offsets from adjacent decoding spheres of said error-correction code until said combinations **fill in all bit positions** corresponding to said data vector such that centers of said adjacent decoding spheres correspond to said index values" [Emphasis Added]. What bit positions are being filled in? Note: bit positions generally refer to the position of a bit in a data stream or a group of data bits, yet nowhere does the claim specify any data stream or a group of data bits related to the bit position.

Claim 20 recites "combines said centers of said adjacent decoding spheres with said center of said central index decoding sphere to form **pairs of indexes**" [Emphasis Added]. The relationship between index values, pairwise combined hash indices in claim and pairs of indices is not clear. Are pairs of indexes the same as pairwise combined hash indices or are the some other index?

Claims 6, 13 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "said combination" in line 13. There is insufficient antecedent basis for this limitation in the claim.

Claim 6 recites "identify all possible offsets from adjacent decoding spheres of said error-correction code until said combinations **fill in all bit positions** corresponding to said data vector such that centers of said adjacent decoding spheres correspond to said index values" [Emphasis Added]. What bit positions are being filled in? Note: bit positions generally refer to the position of a bit in a data stream or a group of data bits, yet nowhere does the claim specify any data stream or a group of data bits related to the bit position.

Claim 13 recites the limitation "said combination" in line 12. There is insufficient antecedent basis for this limitation in the claim.

Claim 13 recites "identify all possible offsets from adjacent decoding spheres of said error-correction code until said combinations **fill in all bit positions** corresponding to said data vector such that centers of said adjacent decoding spheres correspond to said index values" [Emphasis Added]. What bit positions are being filled in? Note: bit positions generally refer to the position of a bit in a data stream or a group of data bits, yet nowhere does the claim specify any data stream or a group of data bits related to the bit position.

Claim 19 recites the limitation "said combination" in line 14. There is insufficient antecedent basis for this limitation in the claim.

Claim 19 recites "identify all possible offsets from adjacent decoding spheres of said error-correction code until said combinations **fill in all bit positions** corresponding to said data vector such that centers of said adjacent decoding spheres correspond to said index values" [Emphasis Added]. What bit positions are being filled in? Note: bit positions generally refer to the position of a bit in a data stream or a group of data bits, yet nowhere does the claim specify any data stream or a group of data bits related to the bit position.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 8-14, 23 and 25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 8, 13 and 14 are abstract methods that can be carried out by hand or in a computer program with no link to any hardware. Abstract method and computer programs are non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 8, 15 and 21-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Arnold; Richard F. et al. (US 4564944 A, hereafter referred to as Arnold).

35 U.S.C. 102(b) rejection of claims 1, 8 and 15.

Arnold teaches an inverse fault-tolerant decoder implemented for an error-correction code (Note: decoding substantially performs the inverse of encoding since decoding extracts data from originally encoded data and hence is substantially the inverse of encoding; in addition, the Decoder in Figure 1 of Arnold is designed to perform the inverse operation of decoding in order to retrieve fault-tolerant data hence is an inverse fault-tolerant decoder) configured to transform a data vector into a plurality of predetermined index values, each of said index values specifying a location within a first address space (the data vector on line 128 in Figures 1 and 3A in Arnold are transformed into Hash indices HF1-HFH whereby H=3 in Figure 3A); combining pairs of said index values to form corresponding pairwise combined hash indices (Figures 3A and 5 in Arnold teach that the combination of HF1-HFH form combined hash indices for looking up data in 4kx16 ROS; in the case that H=2 the pair HF1-HF2 form a pairwise combined hash indices for looking up data in a pair of 4kx16 ROS), each of said pairwise combined hash indices specifying a location within a second address space, said second address space being greater than said first address space (in the case that H=2 the pair HF1-HF2 form a pairwise combined

hash indices for looking up data in a pair of 4kx16 ROS whereby the size of the Address space for the pair HF1-HF2 is 2 times the size of the Address space for either HF1 or HF2); and data storage configured as a hash table addressable throughout said second address space, said hash table referencing indexed data corresponding to said combined hash indices (in the case that H=2 the pair HF1-HF2, a pair of 4kx16 ROS form a data storage configured as a hash table addressable throughout said second address space, said hash table referencing indexed data corresponding to said combined hash indices).

35 U.S.C. 102(b) rejection of claims 21, 23 and 25.

In the case that H=2 the pair HF1-HF2 in Figure 5 of Arnold, the pair HF1-HF2 are in lexicographical order.

35 U.S.C. 102(b) rejection of claims 22, 24 and 26.

In the case that H=2 the pair HF1-HF2 in Figure 5 of Arnold, the pair HF1-HF2 are substantially concatenated in lexicographical order.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 2-7, 9-14 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arnold; Richard F. et al. (US 4564944 A, hereafter referred to as Arnold) in view of Berkovich et al. (Berkovich, S., El-Qawasmeh, E., "Reversing the Error-Correction Scheme for a Fault-Tolerant Indexing, " The Computer Journal, vol. 43, no. 1, pp. 54 - 64, January 2000).

35 U.S.C. 103(a) rejection of claims 2, 9 and 16.

Arnold substantially teaches the claimed invention described in claims 1, 8 and 15 (as rejected above).

However Arnold does not explicitly teach the specific use of bit-attribute data.

Berkovich et al. (hereafter referred to as Berkovich), in an analogous art, teaches that the data vectors used in an inverse fault-tolerant decoder are comprised of bit-attribute data (see col. 1, page 1 of Berkovich). The Examiner asserts that Arnold teaches an inverse fault-tolerant decoder for digital data and Berkovich teaches an inverse fault-tolerant decoder for a specific type of digital data comprising bit-attribute data. One of ordinary skill in the art at the time the invention was made would have recognized that the digital data comprising bit-

attribute data in Berkovich is digital data that the inverse fault-tolerant decoder in Arnold was designed to decode.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Arnold with the teachings of Berkovich by using the fault-tolerant decoder in Arnold on a type of digital data for which it was designed such as bit-attribute data. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the fault-tolerant decoder in Arnold on a type of digital data for which it was designed such as bit-attribute data would have provided a fault-tolerant environment for a specific type of data for which the fault-tolerant decoder in Arnold was designed.

35 U.S.C. 103(a) rejection of claims 3, 4, 10, 11 and 17.

Col. 2 on page 6 of Berkovich teaches a Golay [23,12,7] code; Note: paragraph [0097] on page 32 of the Applicant's specification teaches that a Golay [23,12,7] code is an example of an inverse error correction code hence a decoder for decoding a Golay [23,12,7] code is an inverse fault-tolerant decoder.

35 U.S.C. 103(a) rejection of claims 5, 12 and 18.

Each of the buckets of a Golay code of Hamming distance 2 comprise border vector types of hamming distance 2 located at a border of a decoding sphere and non-border vector types of Hamming distance less than 2 located interior to said decoding sphere.

35 U.S.C. 103(a) rejection of claims 6, 13 and 19.

Arnold teaches an inverse fault-tolerant decoder implemented for an error-correction code (Note: decoding substantially performs the inverse of encoding since decoding extracts data from originally encoded data and hence is substantially the inverse of encoding; in addition, the Decoder in Figure 1 of Arnold is designed to perform the inverse operation of decoding in order to retrieve fault-tolerant data hence is an inverse fault-tolerant decoder) configured to transform a data vector into a plurality of predetermined index values, each of said index values specifying a location within a first address space (the data vector on line 128 in Figures 1 and 3A in Arnold are transformed into Hash indices HF1-HFH whereby H=3 in Figure 3A); combining pairs of said index values to form corresponding pairwise combined hash indices (Figures 3A and 5 in Arnold teach that the combination of HF1-HFH form combined hash indices for looking up data in 4kx16 ROS; in the case that H=2 the pair HF1-HF2 form a pairwise combined hash indices for looking up data in a pair of 4kx16 ROS), each of said pairwise combined hash indices specifying a location within a second address space, said second address space being greater than said first address space (in the case that H=2 the pair HF1-HF2 form a pairwise combined hash indices for looking up data in a pair of 4kx16 ROS whereby the size of the Address space for the pair HF1-HF2 is 2 times the size of the Address space for either HF1 or HF2); and data storage configured as a hash table addressable throughout said second address space, said hash table referencing indexed data

corresponding to said combined hash indices (in the case that H=2 the pair HF1-HF2, a pair of 4kx16 ROS form a data storage configured as a hash table addressable throughout said second address space, said hash table referencing indexed data corresponding to said combined hash indices).

However Arnold does not explicitly teach the specific use of bit-attribute data. Berkovich et al. (hereafter referred to as Berkovich), in an analogous art, teaches that the data vectors used in an inverse fault-tolerant decoder are comprised of bit-attribute data (see col. 1, page 1 of Berkovich). The Examiner asserts that Arnold teaches an inverse fault-tolerant decoder for digital data and Berkovich teaches an inverse fault-tolerant decoder for a specific type of digital data comprising bit-attribute data. One of ordinary skill in the art at the time the invention was made would have recognized that the digital data comprising bit-attribute data in Berkovich is digital data that the inverse fault-tolerant decoder in Arnold was designed to decode. Note also that the recitation "identify all possible offsets from adjacent decoding spheres of said error-correction code until said combinations fill in all bit positions corresponding to said data vector such that centers of said adjacent decoding spheres correspond to said index values", in claims 6, 13 and 19 appears to be an abstract description of a Golay code, which is inherently encompassed by a Golay code.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Arnold with the teachings of Berkovich by using the fault-tolerant decoder in Arnold on a type of digital data for which it was designed such as bit-attribute data. This modification would have been obvious

to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the fault-tolerant decoder in Arnold on a type of digital data for which it was designed such as bit-attribute data would have provided a fault-tolerant environment for a specific type of data for which the fault-tolerant decoder in Arnold was designed.

35 U.S.C. 103(a) rejection of claims 7, 14 and 20.

Arnold teaches an inverse fault-tolerant decoder implemented for an error-correction code (Note: decoding substantially performs the inverse of encoding since decoding extracts data from originally encoded data and hence is substantially the inverse of encoding; in addition, the Decoder in Figure 1 of Arnold is designed to perform the inverse operation of decoding in order to retrieve fault-tolerant data hence is an inverse fault-tolerant decoder) configured to transform a data vector into a plurality of predetermined index values, each of said index values specifying a location within a first address space (the data vector on line 128 in Figures 1 and 3A in Arnold are transformed into Hash indices HF1-HFH whereby H=3 in Figure 3A); combining pairs of said index values to form corresponding pairwise combined hash indices (Figures 3A and 5 in Arnold teach that the combination of HF1-HFH form combined hash indices for looking up data in 4kx16 ROS; in the case that H=2 the pair HF1-HF2 form a pairwise combined hash indices for looking up data in a pair of 4kx16 ROS), each of said pairwise combined hash indices specifying a location within a second address space, said second address space being greater than said first

address space (in the case that H=2 the pair HF1-HF2 form a pairwise combined hash indices for looking up data in a pair of 4kx16 ROS whereby the size of the Address space for the pair HF1-HF2 is 2 times the size of the Address space for either HF1 or HF2); and data storage configured as a hash table addressable throughout said second address space, said hash table referencing indexed data corresponding to said combined hash indices (in the case that H=2 the pair HF1-HF2, a pair of 4kx16 ROS form a data storage configured as a hash table addressable throughout said second address space, said hash table referencing indexed data corresponding to said combined hash indices).

However Arnold does not explicitly teach the specific use of bit-attribute data. Berkovich et al. (hereafter referred to as Berkovich), in an analogous art, teaches that the data vectors used in an inverse fault-tolerant decoder are comprised of bit-attribute data (see col. 1, page 1 of Berkovich). The Examiner asserts that Arnold teaches an inverse fault-tolerant decoder for digital data and Berkovich teaches an inverse fault-tolerant decoder for a specific type of digital data comprising bit-attribute data. One of ordinary skill in the art at the time the invention was made would have recognized that the digital data comprising bit-attribute data in Berkovich is digital data that the inverse fault-tolerant decoder in Arnold was designed to decode. Note also that the recitation "combines said centers of said adjacent decoding spheres with said center of said central index decoding sphere to form pairs of indexes", in claims 6, 13 and 19 appears to be an abstract description of a Golay code, which is inherently encompassed by a Golay code.

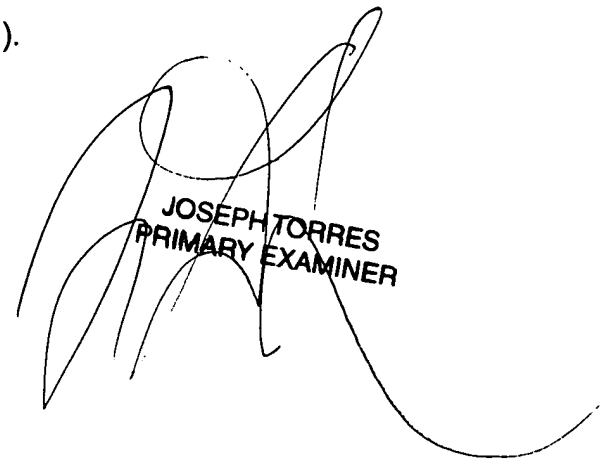
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Arnold with the teachings of Berkovich by using the fault-tolerant decoder in Arnold on a type of digital data for which it was designed such as bit-attribute data. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the fault-tolerant decoder in Arnold on a type of digital data for which it was designed such as bit-attribute data would have provided a fault-tolerant environment for a specific type of data for which the fault-tolerant decoder in Arnold was designed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133